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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/398,689	09/20/1999	ARMIN MRASEK	GR98P2610	1397

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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2189	17

DATE MAILED: 11/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/398,689	MRASEK, ARMIN	
	Examiner	Art Unit	
	Christopher E. Lee	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the After Final Amendment filed on 18th of August 2003. Claims 1, 3 and 5 have been amended; no claim has been canceled; and no claim has been newly added since the Office Action was mailed on 18th of March 2003.

2. Receipt is acknowledged of the request filed on 11th of September 2003 for a Request for Continued Examination (RCE) under 37 CFR 1.114 based on the Application No. 09/398,689, which the request is acceptable and an RCE has been established. Currently, claims 1-6 are pending in this application.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1, 2, 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [hereinafter AAPA] in view of Ugajin et al. [US 5,046,039; hereinafter Ugajin].

Referring to claim 1, AAPA discloses an improved ISDN-data transmission method for transmitting digital data divided up into HDLC data frames of variable lengths from a first data bus to a second data bus operated asynchronously with respect to said first data bus and controlled by a microprocessor (See the preamble of this claim, which is a Jepson-type claim, is impliedly admitted to be old in the art. See MPEP 2129 *Admission as Prior Art*), said improvement which comprises: writing said digital data from said first data bus to a memory having a fixed size (See page 2, lines 10-11; i.e., wherein in fact that an output signal from the HDLC receiver logic unit is supplied to a FIFO memory implies that said digital data is written from said first data bus to said memory); informing said microprocessor, in a form of an interrupt (See page 9, line 25) generated by a memory control unit (i.e., HDLC receiver), if said memory is full or an end of a data frame has been reached (See page 9, line 26 through page 10, line

1); reading via said microprocessor said digital data from said memory (See page 2, lines 11-12; i.e., wherein in fact that a microprocessor removes the data contained in the FIFO memory implies that said microprocessor reads said digital data from said memory); and transmitting from said microprocessor to said memory control unit an acknowledgment of a reception of a data block of said digital data (See Fig. 6A and B).

AAPA does not disclose said memory having a settable size; determining via said microprocessor from said memory control unit a quantity of said digital data to be read from said memory; and setting via said microprocessor a size of said memory.

Ugajin discloses a buffer management system, wherein a memory (i.e., receiver buffer area 78b of Fig. 2) having a settable size (See col. 2, lines 1-12); determining (i.e., decision block in Fig. 3) via a microprocessor (i.e., means for executing software sequence of Fig. 3; See col. 3, lines 24-27 and col. 4, lines 4-8) from a memory control unit (i.e., LLC protocol unit 67 of Fig. 2) a quantity of digital data to be read from said memory (i.e., traffic flow of receiving data; See Fig. 5 and col. 4, lines 27-31); and setting (See block for "setting transmitter/receiver buffer length corresponding to initial value setting table" in Fig. 3) via said microprocessor (i.e., means for executing software sequence of Fig. 3) a size (i.e., new receiver buffer area length) of said memory (i.e., receiver buffer area).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of managing reception buffer, as disclosed by Ugajin, in said method for transmitting digital data, as disclosed by AAPA, for the advantage of preventing the deterioration in the communication performance by changing said memory size (i.e., receiver buffer area size; See Ugajin, col. 1, lines 8-14).

Referring to claim 2, AAPA discloses supplying said digital data from said first data bus (See Fig. 6A and 6B) to a high-level data link control logic unit (i.e., HDLC control device; See page 2, lines 7-8) which checks whether said digital data has been received correctly (See page 1, line 25 through page

2, line 1 and lines 7-9; i.e., wherein in fact HDLC control device checks the data protection information implies that said HDLC logic unit checks whether said digital data has been received correctly) before said digital data is written to said memory (See page 2, lines 7-8; i.e., wherein in fact that an incoming D-channel signal is supplied to an HDLC receiver logic unit implies that said digital data (i.e., HDLC signal) has been received before said digital data is written to said memory).

Referring to claim 5, AAPA discloses a configuration (i.e., network interface equipment for ISDN; See page 1, lines 25-26) for performing an ISDN-data transmission method for transmitting digital data divided up into HDLC data frames of variable length from a first data bus to a second data bus operated asynchronously with respect to said first data bus and controlled and read by a microprocessor (See the preamble of claim 1 in a Jepson-type claim, which is impliedly admitted to be old in the art. See MPEP 2129 *Admission as Prior Art*), said configuration comprising: a memory (i.e., a FIFO memory) having a fixed size for storing data received from said first data bus (See page 2, line 9-12); a control device (i.e., HDLC receiver) for controlling access operations (i.e., informing said microprocessor, in a form of an interrupt generated by said control device; See page 9, line 24 through page 10, line 1) to said memory by said first data bus and said microprocessor (See Fig. 6A and 6B).

AAPA does not disclose said memory having a variable size; and a first, a second registers.

Ugajin discloses a buffer management system, wherein a memory (reception buffer 78b of Fig. 2) having a variable size (See page 282, paragraph right-top, lines 7-16); a first register (i.e., initial setting value table 74 of Fig. 4) storing a value (i.e., reception buffer length 73 of Fig. 4) representing a present size of said memory (i.e. reception buffer), said value being variable in each read cycle of said microprocessor (See Fig. 3 and page 284, paragraph right-bottom, lines 2-9); and a second register (i.e., transmission/ reception buffer ratio table 80 of Fig. 5) storing a quantity of said data just written to said memory (i.e., traffic flow of receiving data; See Fig. 5 and page 283, paragraph left-bottom, lines 19-20).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said dynamic buffer management system, as disclosed by Ugajin, in said configuration, as disclosed by AAPA, for the advantage of preventing the deterioration in the communication performance by changing said memory size (i.e., reception buffer size; See page 281, paragraph right, lines 1-5 of Ugajin).

Referring to claim 6, AAPA discloses a high-level data link control HDLC logic unit (i.e., HDLC control device) connected between said first data bus and said memory (See page 2, lines 7-11).

5. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Ugajin [US 5,046,039] and Chee et al [US 5,673,416; hereinafter Chee].

Referring to claim 3, AAPA discloses an improved ISDN-data transmission method for transmitting digital data divided up into HDLC data frames of variable lengths from a first data bus, controlled by a microprocessor, to a second data bus operated asynchronously with respect to said first data bus (See the preamble of this claim, which is a Jepson-type claim, is impliedly admitted to be old in the art. See MPEP 2129 *Admission as Prior Art*), said improvement which comprises: writing said digital data from said first data bus to a memory having a fixed size (See page 2, lines 10-11; i.e., wherein in fact that an output signal from the HDLC receiver logic unit is supplied to a FIFO memory implies that said digital data is written from said first data bus to said memory); and informing said microprocessor, in a form of an interrupt (See page 9, line 25) generated by a memory control unit (i.e., HDLC receiver), if said memory is full or an end of a data frame has been reached (See page 9, line 26 through page 10, line 1).

AAPA does not disclose said memory having a settable size.

Ugajin teaches a buffer management system, wherein a memory (i.e., receiver buffer area 78b of Fig. 2) having a settable size (See col. 2, lines 1-12).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have substituted said reception buffer, as disclosed by Ugajin, for said memory, as disclosed by AAPA, for the advantage of preventing the deterioration in the communication performance by changing said memory size (i.e., receiver buffer area size; See Ugajin, col. 1, lines 8-14).

AAPA, as modified by Ugajin, does not disclose performing one of informing said microprocessor, in a form of said interrupt generated by said memory control unit, if said memory is ready to accept new data from said first data bus, and said microprocessor asking said memory control unit if said memory is ready to accept said new data from said first data bus; and writing via said microprocessor said new data to said memory.

Chee discloses a memory request and control unit, wherein performing one of informing a microprocessor (i.e., display FIFO module 12 of Fig. 2), in a form of interrupt (i.e., DispDataAck from DRAM controller sequencer 22 to display FIFO module 12 in Fig. 3) generated by a memory control unit (i.e., DRAM controller sequencer 22 of Fig. 3), if a memory (i.e., DRAM 24 of Fig. 3) is ready to accept new data (See col. 9, lines 20-23), and said microprocessor (i.e., display FIFO module) asking (i.e., a low priority request DispLoReq in Fig. 3) said memory control unit (i.e., DRAM controller sequencer) if said memory is ready to accept said new data. (See col. 10, lines 55-57); writing via said microprocessor said new data to said memory (See col. 9, lines 58-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method of memory request and control unit, as disclosed by Chee, in said method, as disclosed by AAPA, as modified by Ugajin, for the advantage of utilizing simple circuit for said microprocessor (i.e., display FIFO module) for efficiently determining when to issue requests for said memory (i.e., DRAM access; See Chee, col. 2, lines 41-43).

AAPA, as modified by Ugajin and Chee, discloses performing one of informing said microprocessor, in a form of said interrupt generated by said memory control unit, if said memory is ready to accept new data

from said first data bus, and said microprocessor asking said memory control unit if said memory is ready to accept said new data from said first data bus; and writing via said microprocessor said new data to said memory (i.e., this limitations are discussed / addressed in the claim 1 rejection); setting (See Ugajin, block for "setting transmitter/receiver buffer length corresponding to initial value setting table" in Fig. 3) via said microprocessor (i.e., means for executing software sequence of Fig. 3; Ugajin) a size (i.e., new receiver buffer area length) of said memory (i.e., receiver buffer area; Ugajin); transmitting from said microprocessor to said memory control unit an acknowledgment of an end of transmission of said new data (See Ugajin, Fig. 6A and B); and placing said new data onto said second data bus (i.e., transmitting digital data (i.e., new data) to a second data bus; See the preamble of this claim, which is a Jepson-type claim, is impliedly admitted to be old in the art. See MPEP 2129 *Admission as Prior Art*).

Referring to claim 4, AAPA discloses supplying said new data (See Fig. 6A and 6B) to a high-level data link control logic unit (i.e., HDLC control device; See page 2, lines 7-8) before it is placed onto the second data bus (See page 2, lines 7-8; i.e., wherein in fact that an incoming D-channel signal is supplied to an HDLC receiver logic unit implies that supplying said new data (i.e., HDLC signal) to a high-level data link control logic unit before it is placed onto the second data bus), said high-level data link control logic unit adding error-checking data (i.e., adding protection information) to said new data (See page 2, lines 16-18).

Response to Arguments

6. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

7. All the arguments, which are drawn to limitations except the newly inserted subject matters, had been discussed/addressed as non-persuasive arguments in the prior Office Action mailed on 18th of March, 2003 and the prior Advisory Action mailed on 2nd of September 2003.

8. The Examiner relied on Ugajin reference (JP 363 292 747 A) in Japanese for the claim rejection. However, the Examiner realizes that there is US patent family document to Ugajin et al. [US 5,046,039], and the Examiner refers to Ugajin et al. [US 5,046,039] as a prior art in the instant Office Action for the convenience of the applicant.

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Christopher E. Lee whose telephone number is 703-305-5950. The Examiner can normally be reached on 9:00am - 5:00pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Christopher E. Lee
Examiner
Art Unit 2189

cel/ CEL

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